ABSTRACT OF THE DISCLOSURE

A method and apparatus for including in a processor instructions for performing horizontal intra-add operations on packed data. One embodiment of the processor is coupled to a memory. The memory has stored therein at least a first packed data. The processor performs operations on data elements in the first packed data to generate a plurality of data elements in a second packed data in response to receiving an instruction. At least two of the plurality of data elements in the second packed data store the results of an intra-add operation, at least one of these results coming from the operation on data elements of the first packed data. One embodiment of a software method utilizes horizontal intra-add instructions for performing butterfly computations as may be employed, for example, in Walsh-Hadamard transforms or in Fast-Fourier Transforms.